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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,104	03/06/2002	James Douglas Wehrly JR.	0254-082/D1	9757

7590

05/29/2003

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EXAMINER

BROCK II, PAUL E


ART UNIT

PAPER NUMBER

2815

DATE MAILED: 05/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/092,104	Applicant(s) WEHRLY, JAMES DOUGLAS	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 April 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 April 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Oath/Declaration

1. The Affidavit under 37 CFR 1.132 filed April 22, 2003 is insufficient to overcome the drawing objection as set forth in the last Office action because: A 132 affidavit is not the appropriate means to overcome a drawing objection. A 132 affidavit may be used “When any claim of an application or a patent under reexamination is rejected or objected to, any evidence submitted to traverse the rejection or objection on a basis not otherwise provided for must be by way of an oath or declaration under this section.” (Emphasis added). Therefore the objection to the drawing is still proper.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the solder containing compound must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: It is not clear in the specification where antecedent basis can be found for the claim term “plural iterations”.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 – 3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. It is not clear in claim 1 if the recitation of “a solder containing compound” in line 8 of the claim is the same “solder containing compound” recited in line 4 of the claim. It is not clear if there are one or two solder containing compounds. How can the same solder containing compound be used in two separate bonds? For purposes of this office action the recitation of “a solder containing compound” in line 12 of the claim will be considered --a second solder containing compound--.

7. It is not clear in claim 1 if the recitation of "solder connections" in line 16 of the claim is the same "solder connections" recited in line 10 of the claim. It is not clear if there are one or two solder connections. How can the same solder connection be used at two different points? For purposes of this office action the recitation of "solder connections" in line 12 of the claim will be considered --second solder connections--.

8. The term "plural iterations" in claim 2 is a relative term which renders the claim indefinite. The term "plural iterations" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is not clear how many iterations "plural iterations" defines. Further, it is not clear how these iterations relate to each other.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1 – 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (USPAT 6133637, Hikita) in view of Sakai et al. (USPAT 5894984, Sakai).

With regard to claim 1, Hikita discloses in figures 43 – 45 a method of creating a stack of integrated circuits selectively connected to provide increased memory density in an application.

Hikita discloses in figures 43 – 45 providing a carrier frame (12) configured to have a plurality of members (12b) emergent into a window within the carrier frame. Hikita discloses in figures 43 – 45 and column 5, lines 10 – 11 applying a solder-containing compound (14c) to the first side of the plurality of members; Hikita discloses in figures 43 – 45 placing a first packaged integrated circuit (14) in contact with the plurality of members. Hikita discloses in figures 43 – 45 and column 21, lines 12 – 14 processing the first integrated circuit and the carrier frame by transfer molding to create solder connections between the plurality of members and the first packaged integrated circuit. It is not clear in Hikita if the transfer molding step includes processing the combination with a heat source. Sakai teaches in figure 8a and column 1, lines 24 – 33 a transfer molding step that includes processing a combination with a heat source. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heat source of Sakai in the transfer molding step of Hikita in order to form an encapsulating member to protect an integrated circuit device. Therefore, the combination of Hikita and Sakai teach processing the first integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the first packaged integrated circuit. Hikita discloses in figures 43 – 45 and column 5, lines 10 – 11 applying a second solder-containing compound (16b) to the second side of the plurality of members of the carrier frame. Hikita discloses in figures 43 – 45 placing a second packaged integrated circuit (16) in contact with the plurality of members. Hikita discloses in figures 43 – 45 and column 21, lines 12 – 14 processing the second integrated circuit and the carrier frame by transfer molding to create second solder connections between the plurality of members and the second integrated circuit. It is not clear in Hikita if the transfer molding step includes processing the combination with a heat source. Sakai

teaches in figure 8a and column 1, lines 24 – 33 a transfer molding step that includes processing a combination with a heat source. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the heat source of Sakai in the transfer molding step of Hikita in order to form an encapsulating member to protect an integrated circuit device.

Therefore, the combination of Hikita and Sakai teach processing the second integrated circuit and the carrier frame with a heat source to create solder connections between the plurality of members and the second packaged integrated circuit.

With regard to claim 2, Hikita discloses in figures 43 – 45 in which plural iterations of the carrier frame are created in a carrier bed.

With regard to claim 3, Hikita discloses in figures 43 – 47 in which the resulting assembly of the carrier frame and the first and second integrated circuits is further processed by separation of the plurality of members from the carrier frame.

Response to Arguments

11. Applicant's arguments filed April 22, 2003 have been fully considered but they are not persuasive.

12. With regard to the applicant's arguments that "to the degree that *Hikita* teaches appending bare die to lead frames and subsequent transfer molding operations, it is inapposite to the present invention," it should be noted that nowhere in Hikita are the integrated circuits referred to as "bare die." Proof that Hikita's integrated circuits are packaged" can be seen in

figure 43 where bond pads 16a are provided at the periphery of the integrated circuit. These bond pads serve the same function as applicant's leads, however are part of a different type of package. Applicant does not define what "packaged integrated circuits" consist of anywhere in the claims. The drawing description of the encapsulated integrated circuit device 26 is not read into the claims. Thus the claims do not define any differences between the integrated circuit packages of Hikita and those of the claimed invention. Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

13. With regard to the applicant's arguments that "Applicant does not understand the Examiner's reference to transfer molding as a suggested commonality to tie the cited references *Hikita* and *Sakai* to the claimed invention," it should be noted that *Sakai* is used to further define the transfer molding step of *Hikita* as a heating step. While it is not clear if the *Sakai* reference is needed to define the heating which occurs in a transfer molding step that is well known in the art, *Sakai* has been provided to make it clear that a transfer molding step does include heating. The rejection has been rewritten and further clarified for easier understanding. Therefore the applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

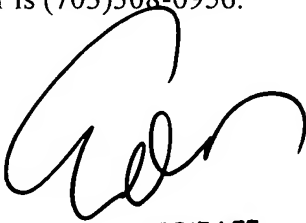
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
May 23, 2003



EDDIE LEE
SUPERVISORY PATENT EXAMINER
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